AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Original) A method for aligning data flows in time division frames, that provides for measuring the phase of said input data flow with respect to the phase of a reference signal, for controlling the delay time introduced by a delay line in said input data flow depending on the measured phase, wherein the phase of the input data flow is measured in a time interval substantially corresponding to the transit time of a sure data sequence containing a logic transition, said sure data sequence being comprised in said input data flow.

2. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 1, wherein the flow of said sure data sequence containing a logic transition is detected, and consequently an enable signal activating a phase sampling operation is generated.

3. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 2, wherein, by said enable signal, a masked reference signal is obtained from the reference signal, said masked reference signal being active only during the passage of the sure data sequence containing a logic transition.

4. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 1, wherein a further delay line is provided with a fixed delay for producing a plurality of delayed phases from the input data flow.

5. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 4, wherein said masked reference signal is used for controlling execution of the sampling operation of said plurality of delayed phases.

6. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 5, wherein a second enable signal is obtained indicating the presence of the logic transition in the sure data sequence containing a logic transition, and said second enable signal is used for activating the sampling operation of said plurality of delayed phases.

7. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 6, wherein said second enable signal is obtained from a correction signal deriving from an alignment operation of the input data flow.

8. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 2, wherein the result of said sampling operation is supplied to a control logic, which generates selection signals ~~apt~~ for controlling the delay time of the delay line, depending on the said result of the sampling operation.

9. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 8, wherein the control logic decides for incrementing or decrementing by one the index i of the selection signals, provided at least one of the first two delayed phases or one of the last two delayed phases in at least one of the values sampled during the whole transit of the sure sequence, differs from an aligned data flow.

10. (*Currently Amended*) The ~~A~~ method for aligning data flows in time division frames[[,]] according to claim 1, wherein said sure data sequence is a frame alignment word and that the time division frames forming the input data flow are either SDH or Sonet frames.

11. (*Currently Amended*) A phase alignment circuit of an input data flow in a time division frame, comprising a phase equalizer ~~apt to equalize~~for equalizing the phase of a reference signal with the phase of the input data flow and drive, through appropriate selection signals, a variable delay line operating on the input data flow, wherein a detector is provided for the transit of a sure data sequence containing a logic transition comprised in the input data flow.

12. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 11, wherein said detector controls the operation of the phase equalizer through an enable signal.

13. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 12, wherein a logic masker is provided for obtaining ~~apt to obtain~~ a masked clock signal from the combination of the enable signal and reference signal.

14. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 11, wherein, downstream of the variable delay line, a further delay line is provided pertaining to the phase equalizer, which produces a plurality of delayed phases from the input data flow.

15. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 14, wherein the phase equalizer comprises a sampler of said plurality of delayed phases, which employ the masked clock signal as a clock signal.

16. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 15, wherein said sampler of said delayed phase plurality receives at least a second enable signal generated by the detector, which indicates the transit of the transition in the sure data sequence.

17. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 15, wherein the phase equalizer comprises a control logic arranged downstream the sampler, for receiving the sampled values of the plurality of delayed phases and emitting the selection signals depending on them.

18. (*Currently Amended*) The ~~A~~ phase alignment circuit of an input data flow in a time division frame[[,]] according to claim 10, wherein the variable delay line is obtained through a ladder of delay elements.

19. (*Withdrawn*) A delay line comprising a plurality of delay elements and a data flow to be delayed passing in series through said plurality of delay elements, wherein one or more of the delay elements also receive the input data flow in parallel, and that said delay elements are apt to select which of the data flows received in series or in parallel should be transmitted.